IN THE CLAIMS

Please substitute the claim set in the appendix entitled Clean Version of Pending Claims for the previously pending claim set. Specific amendments to individual claims are detailed in the following marked up set of claims.

Please amend the claims as follows:

20. (Once Amended) The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with [a surface in the trench that is roughened by an anodic etch] an anodic-etch-roughened surface.

21. (Once Amended) The memory cell of claim 17, wherein the second plate of the trench capacitor comprises the substrate with a [surface in the trench that is roughened by a phosphoric etch] phosphoric-acid-etch-roughened surface.

23. (Once Amended) The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon includes a phosphoric-acid-etch-roughened surface [roughened by etching the surface of the polysilicon with phosphoric acid].

24. (Once Amended) The memory cell of claim 22, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface in the trench, wherein the layer of polysilicon includes an anodic-etch-roughened surface [roughened by etching the surface of the polysilicon with an anodic etch] .

25. (Once Amended) The memory cell of claim 22, wherein the [polycrystalline semiconductor] plate comprises polysilicon.

26. (Once Amended) A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon and a second plate of the trench capacitor [is] disposed adjacent to the first plate;

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

C2 cont'd.

27. (Once Amended) The memory device of claim 26, wherein the [first plate comprises a single crystalline silicon] source/drain region [of a vertical transistor with] comprises a layer of polysilicon formed on [its] a surface in the trench [, wherein the layer of polysilicon is] and includes a phosphoric-acid-etch-roughened [roughened by etching the] surface [of the polysilicon with phosphoric acid].

28. (Once Amended) The memory device of claim 26, wherein the [first plate comprises a single crystalline silicon] source/drain region [of a vertical transistor with] comprises a layer of polysilicon formed on [its] a surface in the trench [, wherein the layer of polysilicon is] and includes an anodic-etch-roughened [roughened by etching the] surface [of the polysilicon with an anodic etch] .

29. (Once Amended) The memory device of claim 26, wherein the [polycrystalline semiconductor] second plate comprises polysilicon.

33. (Once Amended) A memory cell, comprising:

a lateral transistor formed in a layer of semiconductor material outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region; and

a trench capacitor formed in a trench and coupled to the first source/drain region;

wherein the trench capacitor includes a polysilicon plate formed in the trench that is coupled to the first source/drain region, a second plate formed by the substrate [with a surface of the substrate] in the trench, the second plate having a phosphoric-acid-etch-roughened surface or an anodic-etch-roughened surface [roughened by etching a polysilicon material on the surface of the substrate with an etching process selected from the group consisting of an anodic etch and a phosphoric acid etch], and an insulator layer that separates the polysilicon plate from the phosphoric-acid-etch-roughened surface or anodic-acid-etch-roughened [roughened] surface of the substrate.

34. (Once Amended) A memory cell, comprising:

a vertical transistor formed outwardly from a substrate, the transistor including a first source/drain region, a body region and a second source/drain region that are vertically aligned, wherein the first source/drain region comprises single crystalline silicon with a layer of polysilicon formed on its surface; and

a trench capacitor with a plate that is formed in a trench that surrounds a roughened surface of the first source/drain region of the transistor;

wherein the roughened surface of the first source/drain region of the transistor is anodic-etch-roughened or phosphoric-acid-etch-roughened [formed by etching the layer of polysilicon using an etch process selected from the group consisting of an anodic etch and a phosphoric acid etch].

35. (Once Amended) A memory device, comprising:

an array of memory cells, each memory cell including an access transistor that is coupled to a trench capacitor wherein a first plate of the trench capacitor includes a micro-roughened surface of porous polysilicon a second plate of the trench capacitor is disposed adjacent to the first plate, <u>further</u> wherein the micro-roughened surface of porous polysilicon is [formed by etching a layer of polysilicon using an etch process selected from the group consisting of an anodic etch and a phosphoric acid etch] <u>anodic-etch-roughened or phosphoric-acid-etch-roughened</u>;

C3 cont'd.

a number of bit lines that are each selectively coupled to a number of the memory cells at a first source/drain region of the access transistor;

a number of word lines disposed substantially orthogonal to the bit lines and coupled to gates of a number of access transistors; and

a row decoder coupled to the word lines and a column decoder coupled to the bit lines so as to selectively access the cells of the array.

Please add the following new claims:

Sub F11

37. (New) The memory cell of claim 31, wherein the first source/drain region is P-doped or N-doped.

C4

38. (New) The memory cell according to claim 33, wherein the first source/drain region is N-doped or P-doped.

sub H17

39. (New) The memory cell according to claim 34, wherein the single crystalline polysilicon is P-doped or N-doped.

Sub F12

40. (New) The memory cell according to claim 35, wherein the portion of the access transistor is P-doped or N-doped.